IN THE CLAIMS

Please amend the claims as follows:

1. (Canceled)

2. (Currently Amended) ~~The system of claim 1,~~ A read-biasing and amplifying system, comprising:

a first read-biasing and amplifying circuit;

a second read-biasing and amplifying circuit; and

a differential amplifier connected between the first circuit and the second circuit;

wherein at least one of the first circuit and the second circuit include:

an input;

an output;

a first load having a node;

a first control device having a control input and a controlled signal output, wherein the control input of the first control device is coupled to the input, and the controlled signal output of the first control device is coupled to the node of the first load;

a second control device having a control input, a controlled signal output, and a signal input, wherein the control input of the second control device is coupled to the controlled signal output of the first control device, the signal input of the second control device is coupled to the input, and the controlled signal output of the second control device is coupled to the output;

a second load having a node, wherein the node of the second load is coupled to the output;

a third control device having a signal input, wherein the signal input of the third control device is coupled to the output;

wherein the second load comprises a fourth control device;

wherein the node of the second load is a signal input of the fourth control device; and

wherein the first load is a fifth control device, a control input of the fourth control device is coupled to a control input of the fifth control device, and a control input of the third control device is coupled to the output.

3. (Currently Amended) ~~The system of claim 1,~~ A read-biasing and amplifying system, comprising:

a first read-biasing and amplifying circuit;

a second read-biasing and amplifying circuit; and

a differential amplifier connected between the first circuit and the second circuit;

wherein at least one of the first circuit and the second circuit include:

an input;

an output;

a first load having a node;

a first control device having a control input and a controlled signal output, wherein the control input of the first control device is coupled to the input, and the controlled signal output of the first control device is coupled to the node of the first load;

a second control device having a control input, a controlled signal output, and a signal input, wherein the control input of the second control device is coupled to the controlled signal output of the first control device, the signal input of the second control device is coupled to the input, and the controlled signal output of the second control device is coupled to the output;

a second load having a node, wherein the node of the second load is coupled to the output;

a third control device having a signal input, wherein the signal input of the third control device is coupled to the output;

a fourth control device including a control input and a controlled signal output;

wherein the second load comprises a fifth control device;

wherein the node of the second load is a signal input of the fifth control device; and

wherein the first load is a sixth control device, the control input of the fourth control device is coupled to a control input of the sixth control device, a control input of the third control

device is coupled to the output, and a the controlled signal output of the fourth control device is coupled to the controlled signal output of the first control device.

4. (Currently Amended) ~~The system of claim 1,~~ A read-biasing and amplifying system, comprising:

a first read-biasing and amplifying circuit;

a second read-biasing and amplifying circuit; and

a differential amplifier connected between the first circuit and the second circuit;

wherein at least one of the first circuit and the second circuit include:

an input;

an output;

a first load having a node;

a first control device having a control input and a controlled signal output, wherein the control input of the first control device is coupled to the input, and the controlled signal output of the first control device is coupled to the node of the first load;

a second control device having a control input, a controlled signal output, and a signal input, wherein the control input of the second control device is coupled to the controlled signal output of the first control device, the signal input of the second control device is coupled to the input, and the controlled signal output of the second control device is coupled to the output;

a second load having a node, wherein the node of the second load is coupled to the output;

a third control device having a signal input, wherein the signal input of the third control device is coupled to the output;

a fourth control device including a control input and a controlled signal output;

wherein the second load comprises a fifth control device;

wherein the node of the second load is a signal input of the fifth control device; and

wherein the first load is a sixth control device, the control input of the fourth control device is coupled to a control input of the sixth control device, a control input of the third control device is coupled to a controlled signal output of the third control device, and the controlled

signal output of the fourth control device is coupled to the controlled signal output of the first control device.

5. (Currently Amended) ~~The system of claim 1,~~ A read-biasing and amplifying system, comprising:

a first read-biasing and amplifying circuit;

a second read-biasing and amplifying circuit; and

a differential amplifier connected between the first circuit and the second circuit;

wherein at least one of the first circuit and the second circuit include:

an input;

an output;

a first transistor including a source and a well both connected to a first voltage, the first transistor including a gate and a drain;

a second transistor including a source and a well both connected to the first voltage, the second transistor including a gate and a drain, wherein the second transistor gate is connected to the first transistor gate and a second voltage;

a third transistor including a source and a well both connected to the first voltage, the third transistor including a gate and a drain both connected to the output;

a fourth transistor including a source connected to the second voltage, a gate connected to the input, and a drain connected the first transistor drain; and

a fifth transistor including a source connected to the input, a gate connected to the fourth transistor drain, and a drain connected to the output.

6. (Currently Amended) ~~The system of claim 1,~~ A read-biasing and amplifying system, comprising:

a first read-biasing and amplifying circuit;

a second read-biasing and amplifying circuit; and

a differential amplifier connected between the first circuit and the second circuit;

wherein at least one of the first circuit and the second circuit include:

an input;

an output;

a first transistor including a source and a well both connected to a first voltage, the first transistor including a gate and a drain;

a second transistor including a source and a well both connected to the first voltage, the second transistor including a gate and a drain, wherein the second transistor gate is connected to the first transistor gate and a second voltage; and

a feedback biasing circuit, wherein the feedback biasing circuit consists of:

a third transistor including a source and a well both connected to the first voltage, the third transistor including a gate and a drain both connected to the output;

a fourth transistor including a source connected to the second voltage, a gate connected to the input, and a drain connected the first transistor drain; and

a fifth transistor including a source connected to the input, a gate connected to the fourth transistor drain, and a drain connected to the output.

7. (Currently Amended) ~~The system of claim 1,~~ A read-biasing and amplifying system, comprising:

a first read-biasing and amplifying circuit;

a second read-biasing and amplifying circuit; and

a differential amplifier connected between the first circuit and the second circuit;

wherein at least one of the first circuit and the second circuit include:

an input;

an output;

quick-charging means for simultaneously raising potentials of a bit line and the output;

a load for a memory device being sensed, and

a feedback means for preventing the potential of the bit line from exceeding a read-bias potential.

8. (Currently Amended) ~~The system of claim 1,~~ A read-biasing and amplifying system, comprising:

a first read-biasing and amplifying circuit;

a second read-biasing and amplifying circuit; and

a differential amplifier connected between the first circuit and the second circuit;

wherein at least one of the first circuit and the second circuit include:

an input;

an output;

quick-charging means for simultaneously raising potentials of a bit line and the output and for continuing to raise the potential of the output when the potential of the bit line is no longer raised;

a load for a memory device being sensed, and

a feedback means for preventing the potential of the bit line from exceeding a read-bias potential.

9. (New) The system of claim 2, wherein the input is connected to a bit line.

10. (New) The system of claim 2, wherein the output is adapted to be operably connected to a microprocessor.

11. (New) The system of claim 2, wherein the input is connected to a bit line, and wherein the output is adapted to be operably connected to a microprocessor.

12. (New) The system of claim 2, wherein at least one of the third, fourth and fifth control devices is a p-channel transistor.

13. (New) The system of claim 2, wherein each of the third, fourth and fifth control devices is a p-channel transistor.

14. (New) The system of claim 2, wherein the first load is a p-channel transistor.

15. (New) The system of claim 2, wherein the first control device and the second control device are both n-channel transistors.

16. (New) The system of claim 3, wherein the input is connected to a bit line.

17. (New) The system of claim 3, wherein the output is adapted to be operably connected to a microprocessor.

18. (New) The system of claim 3, wherein the input is connected to a bit line, and wherein the output is adapted to be operably connected to a microprocessor.

19. (New) The system of claim 3, wherein at least one of the third, fourth and sixth control devices is a p-channel transistor.

20. (New) The system of claim 3, wherein each of the third, fourth and sixth control devices is a p-channel transistor.

21. (New) The system of claim 3, wherein the first load is a p-channel transistor.

22. (New) The system of claim 3, wherein the first control device and the second control device are both n-channel transistors.

23. (New) The system of claim 4, wherein the input is connected to a bit line.

24. (New) The system of claim 4, wherein the output is adapted to be operably connected to a microprocessor.

25. (New) The system of claim 4, wherein the input is connected to a bit line, and wherein the output is adapted to be operably connected to a microprocessor.

26. (New) The system of claim 4, wherein at least one of the third, fourth and sixth control devices is a p-channel transistor.

27. (New) The system of claim 4, wherein each of the third, fourth and sixth control devices is a p-channel transistor.

28. (New) The system of claim 4, wherein the first load is a p-channel transistor.

29. (New) The system of claim 4, wherein the first control device and the second control device are both n-channel transistors.

30. (New) The system of claim 5, wherein at least one of the first transistor, second transistor, and third transistor is a p-channel transistor.

31. (New) The system of claim 5, wherein at least one of the third transistor and fourth transistor is an n-channel transistor.

32. (New) The system of claim 5, wherein the first, second and third transistors are p-channel transistors, and the fourth and fifth transistors are n-channel transistors.

33. (New) The system of claim 5, wherein the first voltage is Vcc.

34. (New) The system of claim 5, wherein the second voltage is Vss.

35. (New) The system of claim 5, wherein the third transistor is a quick-charging device adapted to operate in a saturated region for quick charging of a bit line and adapted to be in an off state during sensing of a bit line.

36. (New) The system of claim 5, wherein the second transistor, during a sensing operation, operates in a linear region and provides current and acts as a load.

37. (New) The system of claim 5, wherein the first transistor, fourth transistor, and third transistor operate as a feedback circuit during a sensing operation.

38. (New) The system of claim 6, wherein at least one of the first transistor, second transistor, and third transistor is a p-channel transistor.

39. (New) The system of claim 6, wherein at least one of the third transistor and fourth transistor is an n-channel transistor.

40. (New) The system of claim 6, wherein the first, second and third transistors are p-channel transistors, and the fourth and fifth transistors are n-channel transistors.

41. (New) The system of claim 6, wherein the first voltage is Vcc.

42. (New) The system of claim 6, wherein the second voltage is Vss.

43. (New) The system of claim 6, wherein the third transistor is a quick-charging device adapted to operate in a saturated region for quick charging of a bit line and adapted to be in an off state during sensing of a bit line.

44. (New) The system of claim 6, wherein the second transistor, during a sensing operation, operates in a linear region and provides current and acts as a load.

45. (New) The system of claim 7, wherein the quick-charging means includes means for continuing to raise the potential of the output when the potential of the bit line is no longer being raised.

46. (New) The system of claim 7, wherein the input is adapted to be operatively coupled to the bit line.

47. (New) The system of claim 7, wherein the output is adapted to be operatively coupled to a microprocessor.

48. (New) The system of claim 7, wherein the quick-charging means is operatively coupled to the input and the output.

49. (New) The system of claim 7, wherein the load is distinct from the quick-charging means.

50. (New) The system of claim 49, wherein the load is a resistive load.

51. (New) The system of claim 50, wherein the resistive load is a p-channel MOSFET.

52. (New) The system of claim 7, wherein the feedback means is operatively coupled to the input.

53. (New) The system of claim 52, wherein the feedback means includes a p-channel MOSFET operatively coupled to a first n-channel MOSFET, and a second n-channel MOSFET operatively coupled to the first n-channel MOSFET.

54. (New) The system of claim 52, wherein the feedback means includes an n-channel MOSFET operatively coupled to a first p-channel MOSFET, and a second p-channel MOSFET operatively coupled to the first p-channel MOSFET.

55. (New) The system of claim 7, wherein said read-biasing and amplifying system further comprises an enable control operatively coupled to the feedback means which prevents the read-biasing and amplifier circuit from sensing the binary state of the memory device being sensed unless the potential of the enable control substantially equals a predetermined enable voltage.

56. (New) The system of claim 7, wherein the quick-charging device comprises a p-channel MOSFET.

57. (New) The system of claim 7, wherein the quick-charging device comprises a n-channel MOSFET.

58. (New) The system of claim 7, wherein the memory device being sensed is a floating gate memory device.

59. (New) The system of claim 7, including a load transistor coupled to the output in parallel to the quick-charging means.

60. (New) The system of claim 7, wherein the feedback circuit consists of three transistors operatively coupled to the input node.

61. (New) The system of claim 60, wherein the three transistors consist of:

a first n-channel transistor coupled in series between the input node and the output node;

a second n-channel transistor coupled between a gate node of the first n-channel transistor and the lower supply voltage node, a gate node of the second n-channel transistor is coupled to the input node; and

a first p-channel transistor couple between the gate node and the first n-channel transistor and the upper supply voltage node.

62. (New) The system of claim 7, including an enable transistor coupled to the feedback circuit.

63. (New) The system of claim 8, wherein the input is adapted to be operatively coupled to the bit line.

64. (New) The system of claim 8, wherein the output is adapted to be operatively coupled to a microprocessor.

65. (New) The system of claim 8, wherein the quick-charging means is operatively coupled to the input and the output.

66. (New) The system of claim 8, wherein the load is distinct from the quick-charging means.

67. (New) The system of claim 66, wherein the load is a resistive load.

68. (New) The system of claim 67, wherein the resistive load is a p-channel MOSFET.

69. (New) The system of claim 8, wherein the feedback means is operatively coupled to the input.

70. (New) The system of claim 69, wherein the feedback means includes a p-channel MOSFET operatively coupled to a first n-channel MOSFET, and a second n-channel MOSFET operatively coupled to the first n-channel MOSFET.

71. (New) The system of claim 69, wherein the feedback means includes an n-channel MOSFET operatively coupled to a first p-channel MOSFET, and a second p-channel MOSFET operatively coupled to the first p-channel MOSFET.

72. (New) The system of claim 8, wherein said read-biasing and amplifying system further comprises an enable control operatively coupled to the feedback means which prevents the read-biasing and amplifier circuit from sensing the binary state of the memory device being sensed unless the potential of the enable control substantially equals a predetermined enable voltage.

73. (New) The system of claim 8, wherein the quick-charging device comprises a p-channel MOSFET.

74. (New) The system of claim 8, wherein the quick-charging device comprises a n-channel MOSFET.

75. (New) The system of claim 8, wherein the memory device being sensed is a floating gate memory device.

76. (New) The system of claim 8, including a load transistor coupled to the output in parallel to the quick-charging means.

77. (New) The system of claim 8, wherein the feedback circuit consists of three transistors operatively coupled to the input node.

78. (New) The system of claim 77, wherein the three transistors consist of:

a first n-channel transistor coupled in series between the input node and the output node;

a second n-channel transistor coupled between a gate node of the first n-channel transistor and the lower supply voltage node, a gate node of the second n-channel transistor is coupled to the input node; and

a first p-channel transistor couple between the gate node and the first n-channel transistor and the upper supply voltage node.

79. (New) The system of claim 8, including, an enable transistor coupled to the feedback circuit.

80. (New) The system of claim 8, wherein the bit line remains operatively coupled to the input when the bit line is discharged.

81. (New) A read-biasing and amplifying system, comprising:

a first read-biasing and amplifying circuit;

a second read-biasing and amplifying circuit; and

a differential amplifier connected between the first circuit and the second circuit;

an input adapted to be operatively coupled to the bit line;

an output adapted to be operatively coupled to a microprocessor;

quick-charging means, operatively coupled to the input and the output, for simultaneously raising potentials of a bit line and the output and for continuing to raise the potential of the output when the potential of the bit line is no longer raised;

a resistive load for a memory device being sensed, wherein the load is distinct from the quick-charging means; and

a feedback means, operatively coupled to the input, for preventing the potential of the bit line from exceeding a read-bias potential, wherein the feedback means includes a p-channel MOSFET operatively coupled to a first n-channel MOSFET, and a second n-channel MOSFET operatively coupled to the first n-channel MOSFET.

82. (New) The circuit of claim 81, wherein the resistive load is a p-channel MOSFET.